

ADG601/ADG602
FEATURES

Low On Resistance 2.5 Ω Max
<0.6 Ω On Resistance Flatness
Dual ± 2.7 V to ± 5.5 V or Single 2.7 V to 5.5 V Supplies
Rail-to-Rail Input Signal Range
Tiny 6-Lead SOT-23 and 8-Lead MSOP Packages
Low Power Consumption
TTL/CMOS Compatible Inputs

APPLICATIONS

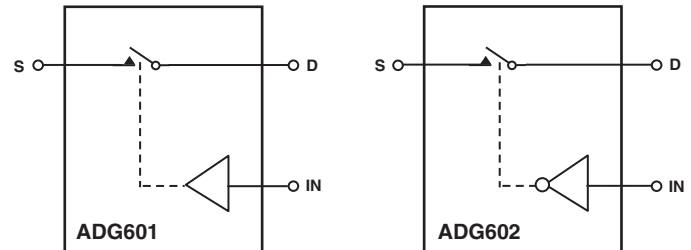
Automatic Test Equipment
Power Routing
Communication Systems
Data Acquisition Systems
Sample and Hold Systems
Avionics
Relay Replacement
Battery-Powered Systems

GENERAL DESCRIPTION

The ADG601/ADG602 are monolithic CMOS SPST (single pole, single throw) switches with on resistance typically less than 2.5 Ω . The low on resistance flatness makes the ADG601/ADG602 ideally suited to many applications, particularly those requiring low distortion. These switches are ideal for replacements for mechanical relays because they are more reliable and have lower power requirements and a much smaller package size.

The ADG601 is a normally open (NO) switch, while the ADG602 is normally closed (NC). Each switch conducts equally well in both directions when ON, with the input signal range extending to the supply rails.

The switches are available in tiny 6-lead SOT-23 and 8-lead MSOP packages.

FUNCTIONAL BLOCK DIAGRAMS


SWITCHES SHOWN FOR A LOGIC 1 INPUT

Table I. Truth Table

| ADG601 In | ADG602 In | Switch Condition |
|-----------|-----------|------------------|
| 0 | 1 | OFF |
| 1 | 0 | ON |

PRODUCT HIGHLIGHTS

1. Low On Resistance (2 Ω typical).
2. Dual ± 2.7 V to ± 5.5 V or Single 2.7 V to 5.5 V Supplies.
3. Tiny 6-lead SOT-23 and 8-lead MSOP Packages.
4. Rail-to-Rail Input Signal Range.

REV. A

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ADG601/ADG602—SPECIFICATIONS

DUAL SUPPLY¹ ($V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.)

| Parameter | B Version | | Unit | Test Conditions/Comments |
|--|----------------------|----------------|-------------------|--|
| | +25°C | -40°C to +85°C | | |
| ANALOG SWITCH | | | | |
| Analog Signal Range | V_{SS} to V_{DD} | | V | $V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$ |
| On Resistance (R_{ON}) | 2 | | Ω typ | $V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$; |
| | 2.5 | 5.5 | Ω max | Test Circuit 1 |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 0.35 | 0.4 | Ω typ | $V_S = \pm 3.3\text{ V}$, $I_S = -10\text{ mA}$ |
| | 0.5 | 0.6 | Ω max | |
| LEAKAGE CURRENTS | | | | |
| Source OFF Leakage I_S (OFF) | ± 0.01 | | nA typ | $V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ |
| | ± 0.25 | ± 1 | nA max | $V_S = +4.5\text{ V}/-4.5\text{ V}$, $V_D = -4.5\text{ V}/+4.5\text{ V}$; |
| Drain OFF Leakage I_D (OFF) | ± 0.01 | | nA typ | Test Circuit 2 |
| | ± 0.25 | ± 1 | nA max | $V_S = +4.5\text{ V}/-4.5\text{ V}$, $V_D = -4.5\text{ V}/+4.5\text{ V}$; |
| Channel ON Leakage I_D , I_S (ON) | ± 0.01 | | nA typ | Test Circuit 2 |
| | ± 0.25 | ± 1 | nA max | $V_S = V_D = +4.5\text{ V}$ or -4.5 V ; |
| | | | | Test Circuit 3 |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | 2.4 | | V min | |
| Input Low Voltage, V_{INL} | 0.8 | | V max | |
| Input Current | | | | |
| I_{INL} or I_{INH} | 0.005 | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | ± 0.1 | μA max | |
| C_{IN} , Digital Input Capacitance | 2 | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | |
| t_{ON} | 80 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 120 | 155 | ns max | $V_S = 3.3\text{ V}$; Test Circuit 4 |
| t_{OFF} | 45 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 75 | 90 | ns max | $V_S = 3.3\text{ V}$; Test Circuit 4 |
| Charge Injection | 250 | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; Test Circuit 5 |
| Off Isolation | -60 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 6 |
| Bandwidth -3 dB | 180 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; Test Circuit 7 |
| C_S (OFF) | 50 | | pF typ | $f = 1\text{ MHz}$ |
| C_D (OFF) | 50 | | pF typ | $f = 1\text{ MHz}$ |
| C_D , C_S (ON) | 145 | | pF typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.001 | | μA typ | $V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ |
| | | 1.0 | μA max | Digital Inputs = 0 V or 5.5 V |
| I_{SS} | 0.001 | | μA typ | Digital Inputs = 0 V or 5.5 V |
| | | 1.0 | μA max | |

NOTES

¹Temperature range is as follows: B Version: -40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SINGLE SUPPLY¹ ($V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.)

| Parameter | B Version | | Unit | Test Conditions/Comments |
|--|-----------------|----------------|-------------------|--|
| | +25°C | -40°C to +85°C | | |
| ANALOG SWITCH | | | | |
| Analog Signal Range | 0 V to V_{DD} | | V | $V_{DD} = 4.5\text{ V}$ |
| On Resistance (R_{ON}) | 3.5 | | Ω typ | $V_S = 0\text{ V}$ to 4.5 V , $I_S = -10\text{ mA}$; |
| | 5 | 8 | Ω max | Test Circuit 1 |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 0.2 | 0.2 | Ω typ | $V_S = 1.5\text{ V}$ to 3.3 V , $I_S = -10\text{ mA}$ |
| | | 0.35 | Ω max | |
| LEAKAGE CURRENTS | | | | |
| Source OFF Leakage I_S (OFF) | ± 0.01 | | nA typ | $V_{DD} = 5.5\text{ V}$ |
| | ± 0.25 | ± 1 | nA max | $V_S = 4.5\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/4.5\text{ V}$; |
| Drain OFF Leakage I_D (OFF) | ± 0.01 | | nA typ | Test Circuit 2 |
| | ± 0.25 | ± 1 | nA max | $V_S = 4.5\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/4.5\text{ V}$; |
| Channel ON Leakage I_D , I_S (ON) | ± 0.01 | | nA typ | Test Circuit 2 |
| | ± 0.25 | ± 1 | nA max | $V_S = V_D = 4.5\text{ V}$ or 1 V ; |
| | | | nA max | Test Circuit 3 |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | 2.4 | | V min | |
| Input Low Voltage, V_{INL} | 0.8 | | V max | |
| Input Current | | | | |
| I_{INL} or I_{INH} | 0.005 | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | ± 0.1 | μA max | |
| C_{IN} , Digital Input Capacitance | 2 | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | |
| t_{ON} | 110 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 220 | 280 | ns max | $V_S = 3.3\text{ V}$; Test Circuit 4 |
| t_{OFF} | 50 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 80 | 110 | ns max | $V_S = 3.3\text{ V}$; Test Circuit 4 |
| Charge Injection | 20 | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; Test Circuit 5 |
| Off Isolation | -60 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 6 |
| Bandwidth -3 dB | 180 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; Test Circuit 7 |
| C_S (OFF) | 50 | | pF typ | $f = 1\text{ MHz}$ |
| C_D (OFF) | 50 | | pF typ | $f = 1\text{ MHz}$ |
| C_D , C_S (ON) | 145 | | pF typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.001 | | μA typ | $V_{DD} = 5.5\text{ V}$ |
| | | 1.0 | μA max | Digital Inputs = 0 V or 5.5 V |

NOTES

¹Temperature range is as follows: B Version: -40°C to +85°C.²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG601/ADG602

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C, unless otherwise noted.)

| | |
|--|--|
| V _{DD} to V _{SS} | 13 V |
| V _{DD} to GND | -0.3 V to +6.5 V |
| V _{SS} to GND | +0.3 V to -6.5 V |
| Analog Inputs ² | V _{SS} - 0.3 V to V _{DD} + 0.3 V |
| Digital Inputs ² | -0.3 V to V _{DD} + 0.3 V |
| | or 30 mA, whichever occurs first |
| Continuous Current, S or D | 100 mA |
| Peak Current, S or D | |
| (Pulsed at 1 ms, 10% Duty Cycle Max) | 200 mA |
| Operating Temperature Range | |
| Industrial (B Version) | -40°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| MSOP Package | |
| θ _{JA} Thermal Impedance | 206°C/W |
| θ _{JC} Thermal Impedance | 44°C/W |
| SOT-23 Package | |
| θ _{JA} Thermal Impedance | 229.6°C/W |
| θ _{JC} Thermal Impedance | 91.99°C/W |
| Lead Temperature, Soldering (10 sec) | 300°C |
| IR Reflow, Peak Temperature | 220°C |

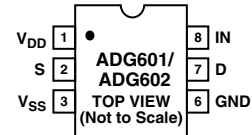
NOTES

¹ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

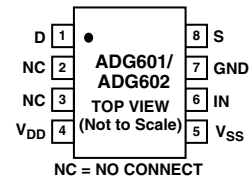
² Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

PIN CONFIGURATIONS

6-Lead SOT-23 (RT-6)



8-Lead MSOP (RM-8)



ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding Information* |
|-----------------|-------------------|--|----------------|-----------------------|
| ADG601BRT-REEL | -40°C to +85°C | Plastic Surface-Mount Package (SOT-23) | RT-6 | STB |
| ADG601BRT-REEL7 | -40°C to +85°C | Plastic Surface-Mount Package (SOT-23) | RT-6 | STB |
| ADG601BRM | -40°C to +85°C | Micro Small Outline Package (MSOP) | RM-8 | STB |
| ADG601BRM-REEL | -40°C to +85°C | Micro Small Outline Package (MSOP) | RM-8 | STB |
| ADG601BRM-REEL7 | -40°C to +85°C | Micro Small Outline Package (MSOP) | RM-8 | STB |
| ADG602BRT-REEL | -40°C to +85°C | Plastic Surface-Mount Package (SOT-23) | RT-6 | SUB |
| ADG602BRT-REEL7 | -40°C to +85°C | Plastic Surface-Mount Package (SOT-23) | RT-6 | SUB |
| ADG602BRM | -40°C to +85°C | Micro Small Outline Package (MSOP) | RM-8 | SUB |
| ADG602BRM-REEL | -40°C to +85°C | Micro Small Outline Package (MSOP) | RM-8 | SUB |
| ADG602BRM-REEL7 | -40°C to +85°C | Micro Small Outline Package (MSOP) | RM-8 | SUB |

*Branding on SOT-23 and MSOP packages is limited to three characters due to space constraints.

CAUTION

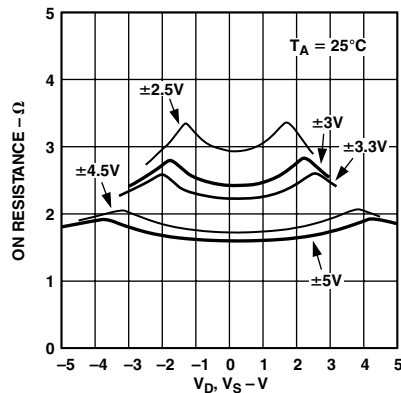
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG601/ADG602 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



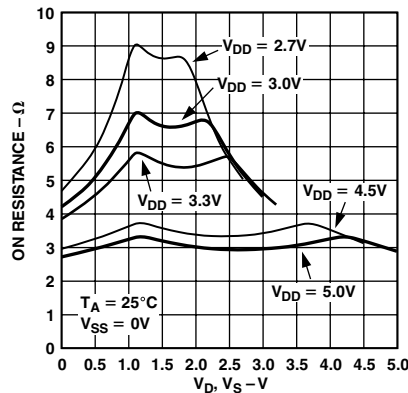
TERMINOLOGY

| | |
|---------------------|---|
| V_{DD} | Most Positive Power Supply Potential. |
| V_{SS} | Most Negative Power Supply Potential. |
| I_{DD} | Positive Supply Current. |
| I_{SS} | Negative Supply Current. |
| GND | Ground (0 V) Reference. |
| S | Source Terminal. May be an input or output. |
| D | Drain Terminal. May be an input or output. |
| IN | Logic Control Input. |
| $V_D (V_S)$ | Analog Voltage on Terminals D, S. |
| R_{ON} | Ohmic Resistance between D and S. |
| $R_{FLAT} (ON)$ | Flatness is defined as the difference between the maximum and minimum values of on resistance as measured over the specified analog signal range. |
| $I_S (OFF)$ | Source Leakage Current with the Switch OFF. |
| $I_D (OFF)$ | Drain Leakage Current with the Switch OFF. |
| $I_D, I_S (ON)$ | Channel Leakage Current with the Switch ON. |
| V_{INL} | Maximum Input Voltage for Logic 0. |
| V_{INH} | Minimum Input Voltage for Logic 1. |
| $I_{INL} (I_{INH})$ | Input Current of the Digital Input. |
| $C_S (OFF)$ | OFF Switch Source Capacitance. Measured with reference to ground. |
| $C_D (OFF)$ | OFF Switch Drain Capacitance. Measured with reference to ground. |
| $C_D, C_S (ON)$ | ON Switch Capacitance. Measured with reference to ground. |
| C_{IN} | Digital Input Capacitance. |
| t_{ON} | Delay between applying the digital control input and the output switching ON. |
| t_{OFF} | Delay between applying the digital control input and the output switching OFF. |
| Charge Injection | A measure of the glitch impulse transferred from the digital input to the analog output during switching. |
| Off Isolation | A measure of unwanted signal coupling through an OFF switch. |
| On Response | Frequency response of the ON switch. |
| Insertion Loss | Loss due to the ON resistance of the switch. |

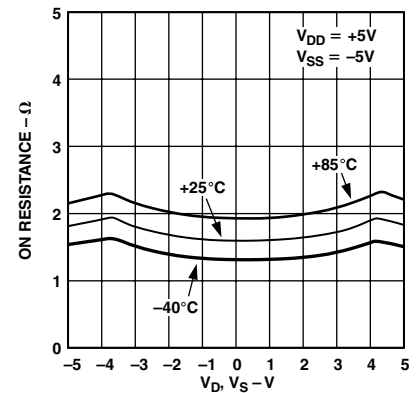
Typical Performance Characteristics



TPC 1. On Resistance vs. $V_D (V_S)$ (Dual Supply)

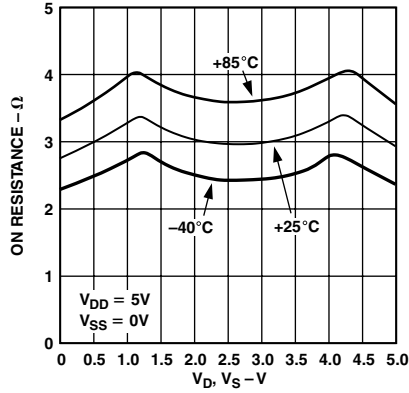


TPC 2. On Resistance vs. $V_D (V_S)$ (Single Supply)

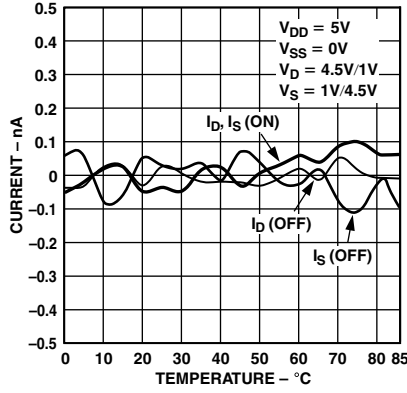


TPC 3. On Resistance vs. $V_D (V_S)$ for Different Temperatures (Dual Supply)

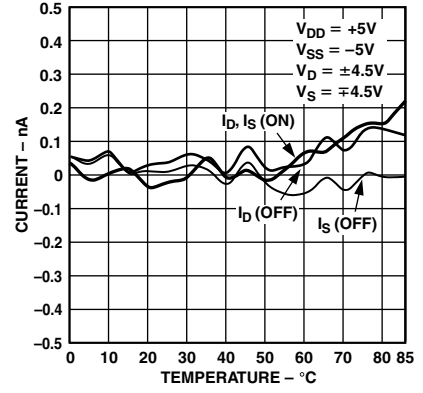
ADG601/ADG602



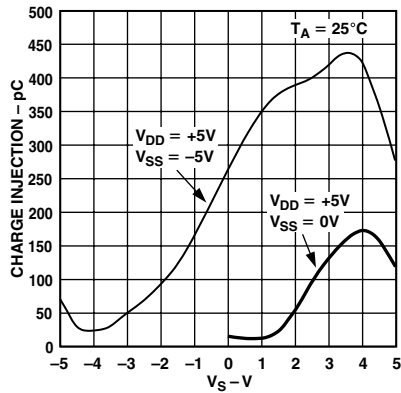
TPC 4. On Resistance vs. V_D (V_S) for Different Temperatures (Single Supply)



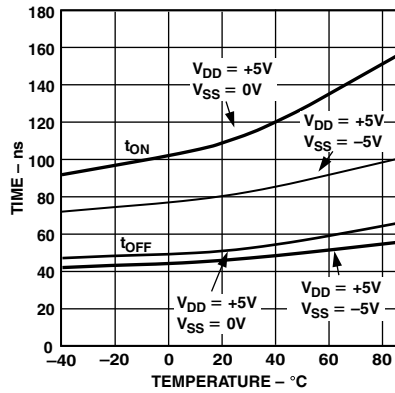
TPC 5. Leakage Currents vs. Temperature (Single Supply)



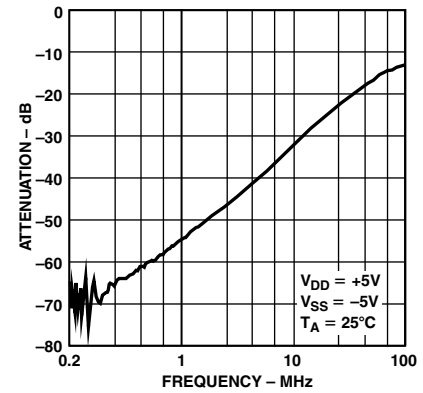
TPC 6. Leakage Currents vs. Temperature (Dual Supply)



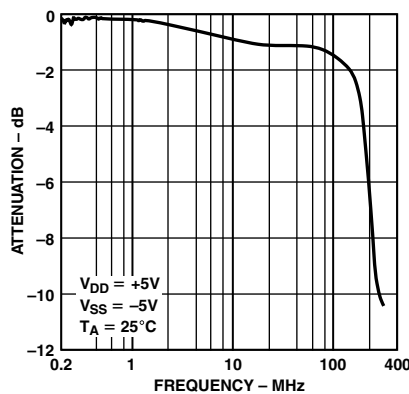
TPC 7. Charge Injection vs. Source Voltage



TPC 8. t_{ON}/t_{OFF} Times vs. Temperature

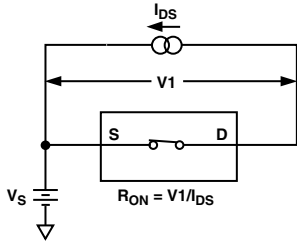


TPC 9. Off Isolation vs. Frequency

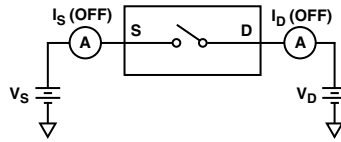


TPC 10. On Response vs. Frequency

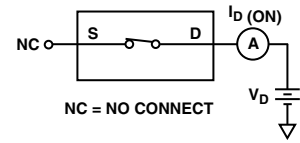
TEST CIRCUITS



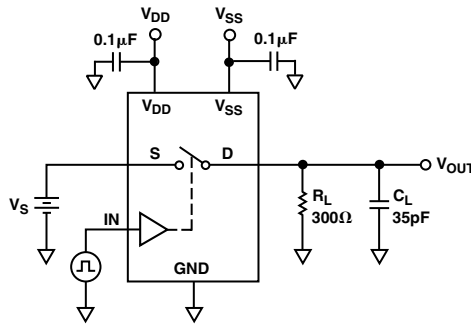
Test Circuit 1. On Resistance



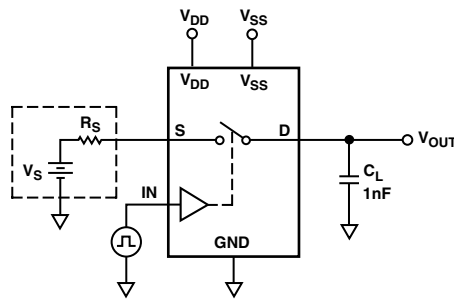
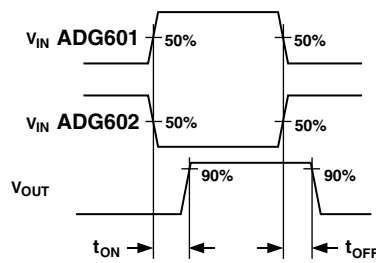
Test Circuit 2. Off Leakage



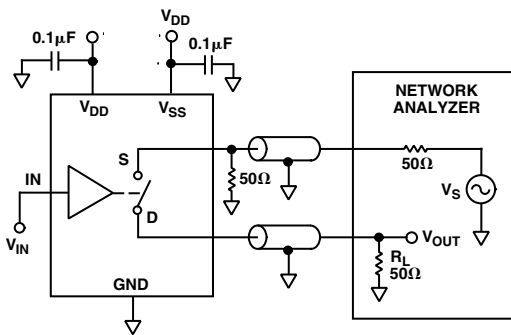
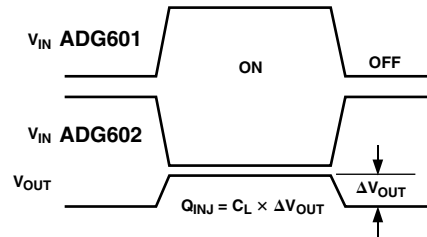
Test Circuit 3. On Leakage



Test Circuit 4. Switching Times

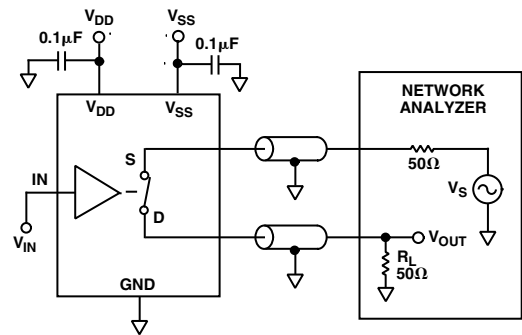


Test Circuit 5. Charge Injection



$$\text{OFF ISOLATION} = 20 \text{ LOG } \frac{V_{\text{OUT}}}{V_S}$$

Test Circuit 6. Off Isolation



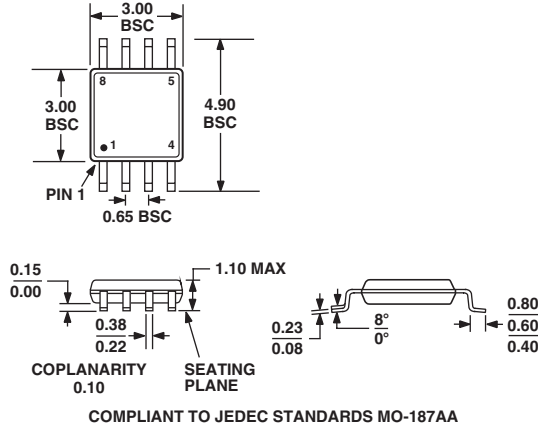
$$\text{INSERTION LOSS} = 20 \text{ LOG } \frac{V_{\text{OUT WITH SWITCH}}}{V_S \text{ WITHOUT SWITCH}}$$

Test Circuit 7. Bandwidth

OUTLINE DIMENSIONS

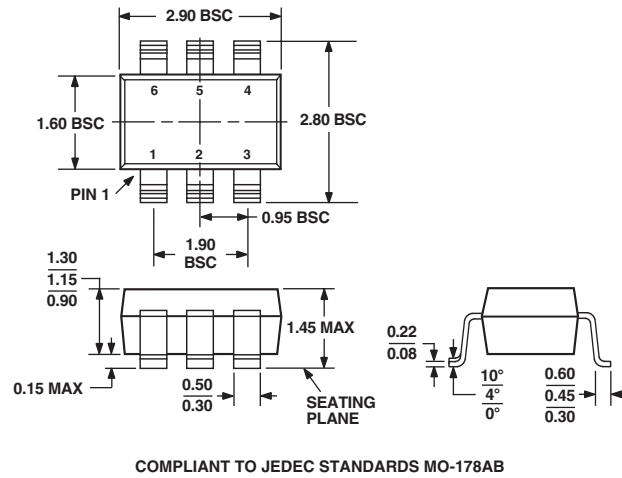
8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters



6-Lead Small Outline Transistor Package [SOT-23]
(RT-6)

Dimensions shown in millimeters



Revision History

| Location | Page |
|---|------|
| 6/03—Data Sheet changed from REV. 0 to REV. A | |
| Changes to SPECIFICATIONS | 2 |
| Updated ORDERING GUIDE | 4 |
| Updated OUTLINE DIMENSIONS | 8 |